In the claims:

1. (currently amended) A semiconductor device, comprising:

a logic circuit, which includes a pair of complementary serially connected MOS transistors coupled between a voltage supply source and a reference voltage source, the transistor coupled to said reference voltage source having a normally higher threshold voltage and lower leakage and driving current than the normal threshold voltage and leakage current of the other of said complementary serially connected MOS transistors in the operational state, and

a bias voltage supply circuit which selectively supplies a first bias voltage in the operational state or a second bias voltage in the standby state which are different from each other to the substrate region of the other of said complementary serially connected MOS transistors with substantially no bias voltage supplied to the substrate region of said transistor coupled to said reference voltage source to raise the threshold voltage and diminish the leakage current of the other of said MOS transistors in the standby state.

2. (previously presented) The semiconductor device of Claim 1, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

3. (canceled)

4. (currently amended) The semiconductor device of Claim 1 ~~3~~, wherein the ~~other of said~~ MOS transistors of the logic circuit is an ~~PMOS~~ NMOS transistor and the other transistor of said logic circuit is a PMOS ~~an NMOS~~ transistor.

5. (canceled)

6. (previously presented) The semiconductor device of Claim 1, wherein one said bias voltage is above the threshold voltage of said other of said complementary serially connected MOS transistors and the other said bias voltage is below the threshold voltage of said other of said complementary serially connected MOS transistors.

7. (previously presented) The semiconductor device of Claim 1, further including at least one additional logic circuit coupled to the bias voltage supply circuit.

8. (currently amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential, the second transistor having a normally lower leakage and driving current than the normal threshold voltage and leakage current of the first MOS transistor ~~the other of said complementary serially connected MOS transistors~~; and

a bias voltage supply circuit which selectively supplies a first bias voltage in the operational state or a second bias voltage in the standby state which are different from each other to the substrate region of the first MOS transistor with substantially no bias voltage supplied to the substrate region of said second transistor to raise the threshold voltage and diminish the leakage current of the first MOS transistor in the steady state.

9. (previously presented) The semiconductor device of Claim 8, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor.

10. (previously presented) The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the second bias voltage.

11. (currently amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential, the second transistor having a normally higher threshold voltage than the normal threshold voltage of said first MOS transistor, and

a bias voltage supply circuit which selectively supplies a first bias voltage in the operational state or a second bias voltage in the standby state which are different from each other to the substrate region of the first MOS transistor with substantially no bias voltage supplied to the substrate region of said transistor coupled to said reference voltage source to raise the threshold voltage and diminish the leakage current of the other of said MOS transistors in the standby state.

12. (currently amended) The semiconductor circuit of Claim 11 ~~8~~, wherein the first bias voltage is lower than the second bias voltage.

13. (previously presented) The semiconductor circuit of Claim 8, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

14. (previously presented) The semiconductor circuit of Claim 13, wherein the MOS transistor of the logic circuit is connected to the first voltage supply line.

15. (currently amended) The semiconductor circuit of Claim 14, wherein the first MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor of the bias voltage supply circuit are PMOS transistors.

16. (currently amended) The semiconductor circuit of Claim 15, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor of the logic circuit and a third voltage supply line.

17 to 27 (canceled)

28 (previously presented) The semiconductor device of claim 11 wherein one of said bias voltages be above the threshold voltage of the first MOS transistor and the other of the bias voltages be below the threshold voltage of said first MOS transistor.